

## CLAIM AMENDMENTS

1 - 10. (canceled)

1           11. (currently amended) The method according to claim  
2 22, further comprising the step of ~~1 characterized by the choice of~~  
3 using selenium, sulfur or tellurium as the chalcogen.

1           12. (currently amended) The method according to claim  
2 22 wherein ~~1 characterized in that~~ the passivation element is im-  
3 planted with a dose of  $10^{12}$  to  $10^{16}$   $\text{cm}^{-2}$ , ~~especially  $10^{14}$  to  $10^{15}$   $\text{cm}^{-2}$ .~~

1           13. (currently amended) The method according to claim  
2 22, further comprising the step of ~~1 characterized in that the~~  
3 selecting metal component of the metal silicide or metal  
4 germanide ~~is selected~~ from the group of cobalt, nickel, titanium,  
5 tungsten ~~[[and/]]~~ or molybdenum.

1           14. (currently amended) The method according to claim  
2 22 wherein ~~1 characterized in that~~ the silicon component of the  
3 silicide as the ~~first layer~~ metal silicide is comprised of  
4 polysilicon or amorphous silicon.

15. (canceled)

1           16. (currently amended) The method according to claim  
2   22, further comprisign the step of 1~~characterized in that~~  
3           providing a mask ~~is arranged~~ on the adjoining layer.

1           17. (currently amended) An electronic component  
2   comprised of at least one passivated metal-semiconductor or metal-  
3   insulator contact made in accordance with claim 22 ~~[[1]]~~.

1           18. (currently amended) A Schottky barrier MOSFET with  
2   an adjustable, especially negative Schottky barrier as the source  
3   ~~[[and/]]~~ or drain contact of an electronic component according to  
4   claim 17.

1           19. (currently amended) A Schottky barrier MOSFET  
2   according to claim 18 ~~characterized in that~~ wherein the contact has  
3   a silicon thickness smaller than 30 nm ~~arranged~~ on an ultra thin  
4   SOI substrate.

1           20. (currently amended) A MOSFET with a gate contact  
2   adjusted by means of passivation as an electronic component  
3   according to claim 17.

1           21. (currently amended) A spin transistor as the  
2   electronic component according to claim 17 ~~characterized in that~~  
3   wherein a semiconductor silicide is selected as the ~~first layer~~

4     metal silicide with Mn or Fe or Co doping for the formation of  
5     magnetic source and drain contacts.

1             22.   (new) A method of making a contact between a first  
2     layer comprised of a metal silicide or metal germanide and a  
3     substrate adjacent the first layer and including silicon or  
4     germanium, the method comprising the steps of:

5             a) incorporating by ion implantation close to a surface  
6     of the substrate or depositing on the surface of the substrate  
7     chalcogen as a passivation element;

8             b) depositing on the substrate or on the chalcogen a  
9     metal component of the first layer to create a structure; and

10            c) thermally treating the structure to form by solid-  
11     state reaction the first layer while simultaneously enriching the  
12     chalcogen by segregation at least at an interface between the first  
13     layer and the substrate to produce the contact.

1             23.   (new) The method defined in claim 22 wherein the  
2     substrate includes Si-Ge-C, Si-C, or Si-Ge.

1           24. (new) A method of making a contact between a first  
2 layer comprised of a metal silicide, metal germanide, or  
3 semiconductor silicide and a substrate adjacent the first layer and  
4 including silicon or germanium, the method comprising the steps of:

5           a) depositing on a surface of the substrate a metal  
6 component of the first layer;

7           b) incorporating by ion implantation close to the surface  
8 of the substrate chalcogen as a passivation element to create a  
9 structure; and

10          c) thermally treating the structure to form by solid-  
11 state reaction the first layer while simultaneously enriching the  
12 chalcogen by segregation at least at an interface between the first  
13 layer and the substrate to produce the contact.

1           25. (new) The method defined in claim 24 wherein step  
2 a) precedes step b).

1           26. (new) The method defined in claim 24 wherein step b)  
2 precedes step a).

1           27. (new) The method defined in claim 24 wherein the  
2 chalcogen is incorporated in the substrate close to the surface.

1           28. (new) The method defined in claim 24 wherein the  
2 chalcogen is incorporated in the metal component close to the  
3 surface.

1           29. (new) The method according to claim 24, further  
2 comprising the step of  
3 using selenium, sulfur or tellurium as the chalcogen.

1           30. (new) The method according to claim 24 wherein the  
2 passivation element is implanted with a dose of  $10^{12}$  to  $10^{16}$   $\text{cm}^{-2}$ .

1           31. (new) The method according to claim 24, further  
2 comprising the step of  
3 selecting metal component of the metal silicide or metal  
4 germanide from the group of cobalt, nickel, titanium, tungsten or  
5 molybdenum.

1           32. (new) The method according to claim 24 wherein the  
2 silicon component of the silicide as the metal silicide is  
3 comprised of polysilicon or amorphous silicon.

1           33. (new) The method according to claim 24, further  
2 comprising the step of  
3 using  $\beta\text{-FeSi}_2$ ,  $\text{Ru}_2\text{Si}_3$ ,  $\text{MnSi}_x$  or  $\text{CrSi}_2$  as a semiconductor  
4 silicide.

5           34. (new) The method according to claim 24, further  
6 comprising the step of  
7           providing a mask on the adjoining layer.

1           35. (new) An electronic component comprised of at least  
2 one passivated metal-semiconductor or metal-insulator contact made  
3 in accordance with claim 24.

1           36. (new) A Schottky barrier MOSFET with an adjustable,  
2 especially negative Schottky barrier as the source or drain contact  
3 of an electronic component according to claim 35.

1           37. (new) A Schottky barrier MOSFET according to claim  
2 36 wherein the contact has a silicon thickness smaller than 30 nm  
3 on an ultra thin SOI substrate.

1           38. (new) A MOSFET with a gate contact adjusted by  
2 means of passivation as an electronic component according to claim  
3 35.

1           39. (new) A spin transistor as the electronic component  
2 according to claim 35 wherein a semiconductor silicide is selected  
3 as the metal silicide with Mn or Fe or Co doping for the formation  
4 of magnetic source and drain contacts.

1                   40.   (new) The method defined in claim 24 wherein the  
2   substrate includes Si-Ge-C, Si-C, or Si-Ge.